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EXAMINER

NGUYEN, TANH Q

ART UNIT PAPER NUMBER

2182

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/871,115

Applicant(s)

APEL ET AL.

Examiner

Tanh Q. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 December 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12-90 is/are pending in the application.
- 4a) Of the above claim(s) 31-55, 72-79 and 81-86 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12-30, 56-71, 80 and 87-90 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 02/10/03, 09/02/04.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 37-55, 72-79 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions (Group I and Group III), there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on August 9, 2004.
2. Applicant's election with traverse of Species I of Group II, directed to claims 12-30, 56-71, 80, 87-90, in the reply filed on 12/06/2004 is acknowledged. The traversal is on the ground(s) that the restriction requirement with respect to Species I and II of Group II is improper because there is no serious burden to the examiner.

Applicant indicated that a thorough search of the apparatus of claims 12-30 will necessitate a search of all devices used in a process control system. This is not found to be persuasive because this is merely applicant's opinion, not fact.

Applicant further indicated that the subject matter of claims 12-30 is not so materially different from that of claims 31-36 to preclude one from searching both the field devices and the I/O devices simultaneously. This is not found to be persuasive because applicant appeared to traverse on the ground that the species are not patentably distinct. If this is the case, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. Thus, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention. If this is not the case, then the species

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are patentably distinct, and a search for the subject matter of claims 31-36 would be required, separately from the search for the subject matter of claims 12-30.

Applicant submitted that a complete search directed to the subject matter of the claims of Group II, Species I would require a search directed to the subject matter of the claims of Group II, Species II, and vice versa. Again, this is not found to be persuasive because this is merely applicant's opinion, not fact.

Applicant also indicated that - because search and examination of the application can be made without a serious burden on the Examiner, it would be wasteful of the time, effort, and resources of both the Applicants and the Patent Office to prosecute claims 12-30 and 56-71 on the one hand, and claims 31-36 on the other hand, in separate applications.

This is not found persuasive because the two species are patentably distinct for the reasons set forth in the restriction requirement. The burden in the examination of multiple species lies in consideration of multiple patentably distinct species in one application. Further, the time, effort and resources of the applicant are not germane to the issue; and the time, effort, and resources of the Patent Office are not wasteful because the two species are not the same.

The requirement is still deemed proper and is therefore made FINAL.

3. Claims 31-36, 81-86 are, therefore, withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species of Group II.
4. Applicant is reminded that upon the cancellation of claims to a non-elected

invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

5. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

6. Claims 16, 17, 23 are objected to because of the following informalities:
“and clock data line” on line 2 of claim 16 should be replaced with “and a clock data line”.

“the device” on line 5 of claim 7 should be replaced with “the I/O device” to be differentiated from the driver device.

“processors” on line 3 of claim 21, line 6 of claim 22, line 2 of claim 23 should be replaced with “processor”.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 12-13, 18-20, 28; 56-57, 62-65; 80, 87-88 are rejected under 35

U.S.C. 102(b) as being anticipated by **Safadi (USP 5,379,278)**.

9. As per claim 12, **Safadi** teaches an input/output (I/O) device [20, FIG. 1; col. 2, lines 18-23] for use in a process control system [10, FIG. 1; col. 2, line 7] for communications in a process control network [11, FIG. 1; col. 2, line 9], the process control system including a plurality of I/O devices [20, 20 A, 20 B] in communication using a bus [14, 14A, FIG. 1; col. 2, lines 8-16], the I/O device comprising:

an interface [50, FIG. 3] for communicatively linking the I/O device with the bus [col. 3, lines 25-28]; and

a device processor [63, 91, FIG. 3] coupled with the interface [col. 3, lines 39-41] for controlling operation of the device [col. 3, lines 35-39 (controlling communication operation of the device); col. 3, lines 52-53] including performing fault detection for the device [col. 4, lines 57-62];

wherein the device processor, upon detection of a potential device fault, severs the communication link provided by the interface with the bus [col. 4, lines 44-52; col. 4, lines 57-62; col. 5, lines 7-10].

10. As per claims 13, 18-20, 28, **Safadi** teaches the bus including a data line and the interface communicatively linking the I/O device with the data line of the bus [col. 3, lines 41-44], and the device processor, upon detection of the potential device fault,

severing the communication link provided by the interface with the data line [col. 4, lines 44-52; col. 4, lines 57-62; col. 5, lines 7-10];

the bus including a plurality of data lines [14A, 14 B, FIG. 2; col. 2, lines 50-53], and the interface communicatively linking the I/O device to the plurality of data lines [FIG. 3], wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the interface with the plurality of data lines of the bus [col. 4, lines 41-43];

the fault detection being an initial fault detection, and further comprising a later fault detection performed by the I/O device after the communicative link from the I/O device and the bus is severed [col. 4, lines 52-67];

the later fault detection being performed in a similar manner to the initial fault detection [col. 4, lines 52-67];

the device processor performing further fault detection upon severing of the communication link, wherein when the device processor detects no device fault from the further fault detection, the device processor reestablishes the communication link with the bus [col. 4, lines 52-67; Abstract];

11. As per claims 56-57, 62-65, Safadi teaches an I/O device comprising a processor that severs a communications link provided by an interface with the bus to a process control system (see rejections to claims 12-13, 18-20, 28 above), hence teaches a method for severing communication between an I/O device and a process control system.

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12. As per claims 80, 87-88, see the rejections to claims 12-13 above.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 14-16, 23-27; 58-60, 66-69; 89-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Safadi** in view of **Yap (USP 6,073,193)**.

15. As per claims 14, 58, 89, Safadi discloses the invention except for a specific relay device coupled between the device processor and the data line of the bus, the relay having a first state communicatively linking the I/O device with the data line, and a second state severing the communicative link between the I/O device and the data line of the bus, wherein the device processor, upon detection of the potential device fault, severs the communication link with the bus by actuating the relay to the second state,.

Yap teaches a relay device [S+, S-, FIG. 2] coupled between the device processor [6, FIG. 2] and the data line of the bus [2a, FIG. 2], the relay having a first state communicatively linking the I/O device [10, FIG. 2] with the data line (connect state), and a second state severing the communicative link between the I/O device and the data line of the bus (disconnect state), wherein the device processor, upon detection

of the potential device fault, severs the communication link with the bus by actuating the relay to the second state [col. 3, line 66-col. 4, line 20; col. 5, lines 63-67].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a relay device, as is taught by Yap, in order to use the relay device to enable the disconnection of the communicative link between the I/O device and the data line of the bus.

16. As per claims 15-16, 59-60, 90, Safadi discloses the invention except for the data line being capable of being affected by the I/O device, and except for the data line being at least one of a transmit data line and a clock data line.

Yap teaches a data line being capable of being affected by the I/O device [col. 5, lines 63-67], and the data line being a transmit data line [D+, D-, FIG. 2].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a data line, such as one being taught by Yap, in order to allow the data line to be affected by the I/O device.

17. As per claims 23-27; 66-69, Safadi discloses the invention except the device processor fault detection including the device processor attempting to affect the bus using the interface, wherein the device processor detects the potential device fault by an inability of the device processor to affect the bus.

Yap teaches the device processor fault detection including the device processor attempting to affect the bus using the interface [col. 5, lines 63-67], wherein the device

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processor detects the potential device fault by an inability of the device processor to affect the bus [brown out condition: col. 5, lines 53-55; col. 1, lines 43-54].

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the device processor fault detection to include the device processor attempting to affect the bus using the interface, as is taught by Yap, in order to allow the data line to be affected by the device processor - upon potential device fault detection.

Yap further teaches the device processor attempting to affect the bus including the device processor attempting to change the state of the bus;

the device processor attempting to change the state of the bus including the device processor forcing a state on the bus [col. 5, lines 63-67];

the device processor forcing the state of the bus including the device processor transmitting one of a digital high value and a digital low value on the bus [col. 3, line 66- col. 4, line 6; col. 4, lines 33-36]; and

the device processor reading the bus after attempting to affect the bus [col. 5, lines 59-63], wherein the device processor determines the inability to affect the bus using the reading of the bus [col. 5, lines 30-34].

18. Claims 17, 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Safadi** in view of **Yap** and **Lee et al. (USP 6,615,301)**.

19. As per claim 17, Safadi teaches the device processor, upon detection of the potential device fault, performing further fault detection on the I/O device and

determining a device fault [col. 4, lines 52-67]. Safadi, therefore, teaches the claimed invention except for a driver device coupled between the device processor and the interface, the driver device having a driver output coupled to the interface and readable by the processor, wherein the device processor performs further fault detection on the device by forcing states to the driver output.

Yap teaches a USB data line [6a, FIG. 1] coupled between the device processor [6, FIG. 1] and an interface [FIG. 4], the data line being readable by the processor [FIG. 1], and device processor forcing states onto the data line [col. 4, lines 14-21].

Lee teaches a driver device driving a USB data signal [col. 5, lines 55-56]. Yap, in combination with Lee, teaches a driver device coupled between the device processor and the interface, the driver device having a driver output coupled to the interface and readable by the processor, wherein the device processor performs further fault detection on the device by forcing states to the driver output.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a driver device, as is taught by Yap and Lee, in order to drive data over the bus.

20. Claims 21-22, 29-30; 70-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Safadi** in view of **AAPA (Applicant Admitted Prior Art - DESCRIPTION OF THE RELATED ART SECTION of Pub. No. 2002/0184410 and [0074])**.

21. As per claims 21-22, Safadi teaches the claimed invention except for the

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potential device fault including the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus, and the device processor severing of the communication link with the bus allowing the other I/O devices to communicate to one another over the bus; and except for the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus including the I/O device affecting the bus by the I/O device transmitting an undesired signal on the data line of the bus.

AAPA teaches a faulty I/O device preventing all other I/O devices on the bus connecting a controller to various I/O devices from communicating with one another and the controller, and causing the bus to go out of service - a condition that poses danger to nearby workers as process activities controlled by the bus may be operating with limited or no control and/or monitoring [[0011] of Pub. No. 2002/0184410] - hence teaches the potential device fault including the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus, and suggests to one of ordinary skill in the art to remove the faulty I/O device from the bus to keep the bus from going out of service and prevent a condition that poses danger to nearby workers.

Safadi teaches the device processor (of I/O device) severing the communication link with the bus upon detection of a potential device fault. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the severance of the communication link, when applied to an faulty I/O device capable causing the bus to go out of service (as is taught by AAPA), would effectively remove the faulty I/O device from the bus in order to keep the bus from going out of service and allow the other I/O devices to communicate to one another over the bus.

AAPA further teaches the faulty I/O device producing an undesirable signal on a bus data line common to all I/O devices on the bus, the undesirable signal prohibiting communication between all I/O devices and the controller on the bus [[0011] of Pub. No. 2002/0184410] - hence teaches the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus (the faulty I/O device) including the I/O device affecting the bus by the I/O device transmitting an undesired signal on the data line of the bus.

22. As per claims 29-30, 70-71, Safadi discloses the invention except for the process control system operating in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising the I/O device being assigned to one of the synchronous time slots, where the device processor performs fault detection during the asynchronous time slot following the corresponding synchronous time slot; and except for the device processor performing the fault detection when the I/O device is not transmitting I/O device information on the bus.

AAPA teaches an I/O device affecting a bus data line (i.e. to perform fault detection) during an asynchronous communication time frame after its corresponding synchronous communication time frame (i.e. the I/O device being assigned to the synchronous communication time frame) within the macro cycle being appreciated by one skilled in the art - where a communication protocol utilizing synchronous and asynchronous communications within macrocycles is used [[0074]]. Likewise, AAPA teaches performing the fault detection when the I/O device is not transmitting I/O device

information on the bus (i.e. I/O device information being transmitted during synchronous time frame, and fault detection being performed during asynchronous time frame following a corresponding synchronous time frame).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the process control system to operate in macrocycles, as is taught by AAPA, in order to allow the device processor to perform fault detection during the asynchronous time slot following the corresponding synchronous time slot (i.e. to perform the fault detection when the I/O device is not transmitting I/O device information on the bus) where a communication protocol utilizing synchronous and asynchronous communications within macrocycles is used - as is known in the art.

23. Claims 29-30, 70-71 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over **Safadi** in view of **Kato et al. (USP 6,397,277)**.

Kato teaches macrocycles [synchronization cycles, FIG. 12] including at least one synchronous time slot [isochronous packets, FIG. 12] and at least one asynchronous time slot [asynchronous packet B, fig. 12] corresponding to the synchronous time slot [within the same synchronization cycle, FIG. 12], and further comprising the I/O device being assigned to one of the synchronous time slots [channels J-N, FIG. 12; col. 8, lines 38-41; col. 9, lines 8-10], the asynchronous time slot following the corresponding synchronous time slot [FIG. 12].

Kato further teaches the synchronous transmission guaranteeing a predetermined amount of data being transmitted within a predetermined time interval

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[col. 9, lines 5-7; col. 9, 9-11; FIG. 12] - hence synchronous transmission being suitable for transmission of data that are generated on a periodic basis; and asynchronous transmission guaranteeing reliable transmission [col. 9, lines 13-16 - as acknowledge and retry signals are normally used to guarantee reliable data transmission], asynchronous transmission being an operation that traditionally takes place as soon as possible [col. 1, lines 57-58], and asynchronous transmission being suitable for non-periodic data transmission.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the process control system to operate in macrocycles, as is taught by Kato, in order to allow transmission of I/O device information (i.e. transmission of data related to the actual process control activities) to be scheduled during synchronous time slots to guarantee transmission within a predetermined time interval - as data related to the actual process control activities are often generated on a periodic basis; and further for the device processor to perform the fault detection during an asynchronous time slot in order to transmit a fault indication, upon detection of a fault, as soon as possible and in a reliable manner.

As above, Kato teaches transmitting I/O device information during a synchronous time slot; and asynchronous transmission being performed by using a time unit not used for synchronous transmission, the asynchronous time slot being used for reliable data transmission and the asynchronous data transmission taking place as soon as possible.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the device processor to use the synchronous time slot and the

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asynchronous time slot for data transmission, as is taught by Kato; and further for the device processor to perform the fault detection during the asynchronous time slot (i.e. when the I/O device is not transmitting I/O device information on the bus) in order to transmit a fault indication, upon detection of a fault, as soon as possible and in a reliable manner.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Quang Nguyen whose telephone number is (703) 305-0138, (or (571) 272-4154 after October 12, 2004) and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (703) 308-3301 (or (571) 272-2100 after October 12, 2004). The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 for After Final, Official, and Customer Services, or (703) 746-5672 (or (571) 273-4154 after October 12, 2004) for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

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03/05/2005

TQN

March 5, 2005